Serial No. 09/873,674
Attorney Docket No. F0537
Firm Reference No. AMDSP0429US

Response to Office Action Dated October 16, 2003
Response Dated January 8, 2004

REMARKS

Claims 1-14, 21-25 and 27 are presently pending.

I. ALLOWABLE SUBJECT MATTER

Applicant acknowledges with appreciation the Examiner's indication that claims 10-14, 24 and 25 are allowable.

II. REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

Claims 1, 4-8, 22, 23 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, U.S. Patent No. 5,600,168 ("Lee") in view of Clevenger et al., U.S. Patent No. 6,509,612 ("Clevenger").[1] Claims 2, 3 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Clevenger as applied to claim 1 and further in view of Mandelman et al., U.S. Patent No. 6,097,070 ("Mandelman"). Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Clevenger as applied to claim 1 and further in view of Liu et al., U.S. Patent No. 6,218,276 ("Liu"). Withdrawal of the rejections is respectfully requested for at least the following reasons.

The applicant respectfully submits a Declaration Under 37 CFR 1.131 showing that he conceived the invention prior to Clevenger et al. and that he diligently reduced it to practice, i.e., constructively by filing the above-identified application with the USPTO on June 4, 2001. Therefore, Clevenger et al. should not be considered prior art to the above-identified application. As Clevenger et al. is not prior art, the other prior art cited in combination with Clevenger et al. do not disclose or suggest all the features of the invention alone or in combination with each other. Thus, claims 1-9, 21-23 and 27 are considered patentable over the prior art of record.

1 The rejection is initially stated on page 2 of the Office Action as being over Lee in view of Hwang, U.S. Patent No. 5,567,966, line 2 of paragraph 2. However, subsequent citations to the secondary reference are to Clevenger, and the column and line citations appear to correspond to Clevenger, rather than Hwang. Therefore the rejection is being treated as a combination of Lee and Clevenger.

III. CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

Any fee(s) resulting from this communication is hereby authorized to be charged to our Deposit Account No. 18-0988; Our Order No. F0537 (AMDSP0429US).

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

Andrew Romero

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Serial No. 09/873,674
Attorney Docket No. F0537
Firm Reference No. AMDSP0429US

Declaration Under 37 CFR 1.131

CERTIFICATE OF MAILING OR FACSIMILE TRANSMISSION UNDER 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is
___ being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Commissioner for Patents address below.
_X_ being transmitted via facsimile to (703) 872-9306 at the U.S. Patent and Trademark Office to the Attention of Examiner Jesse A. Fenty.

Linda McElroy — 1-8-2004
Linda McElroy — Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant:	Zoran Krivokapic	Art Unit:	2815
Serial No:	09/873,674	Examiner:	Jesse A. Fenty
Filing Date:	June 4, 2001	Confirmation No:	5266

Title: **STRADDLED GATE FDSOI DEVICE**

Mail Stop AF: Expedited Procedure
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop AF
EXPEDITED
PROCEDURE

DECLARATION UNDER 37 CFR 1.131

Dear Sir

I, Zoran Krivokapic, depose and state:

1. I am the sole inventor of all claims (i.e., claims 1-14, 21-25 and 27) of the above-identified patent application.

Serial No. 09/873,674
Attorney Docket No. F0537
Firm Reference No. AMDSP0429US

Declaration Under 37 CFR 1.131

2. Prior to May 4, 2001, I conceived the idea of using a straddled gate in a semiconductor device as described and claimed in my application. As evidence of such conception, I filled out and signed an AMD Invention Disclosure TLD ID# F0537 describing the invention (copy attached hereto).

3. During the four weeks between from just prior to May 4, 2001 and the June 4, 2001 filing date of the present application, I worked diligently through my undersigned attorneys to finalize and file the present application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and such willful false statements may jeopardize the validity of the application or any patent issued therefrom.

Signed: _____ Date: Jan. 7th 2004

Zoran Krivokapic

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AR, MDG

[redacted]

TDG--SOI PATENT HARVESTING SESSION
TOPIC: SOI DEVICES
Technical Leader: Srinath Krishnan
GROUP 1--ROOM C-3

1-29

PRIORITY
A ___ B ✓
C ___ D ___

AMD INVENTION DISCLOSURE TLD ID# F0537 Rec'd date ________
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

F0537

Project: ☐, **Product:** ☐, **Process:** ☐, **Technology** ☐, **to which the invention applies (*identify*):**

List 2 to 5 key words useful to search by to find patents or art related to this invention:

Working title of invention: Straddled gate FDSOI device

INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE (1A)

Inventor's signature : ________ **date :** [redacted]
Inventor's printed full name: ZORAN KRIVOKAPIC **Citizenship:** ________
Employee #: ____ **Extension:** ____ **Mail stop:** ____ **Home telephone:(** **)** ____
Division: ____ **Directorate:** ____ **Dept #:** ____ **Dept :** ____ **Manager:** ____
Residence address: ________
Post Office address: ________

Co-Inventor's signature : ________ **date :** ________
Co-Inventor's printed full name: ________ **Citizenship:** ________
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Division: ____ **Directorate:** ____ **Dept #:** ____ **Dept :** ____ **Manager:** ____
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Co-Inventor's signature : ________ **date :** ________
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Division: ____ **Directorate:** ____ **Dept #:** ____ **Dept :** ____ **Manager:** ____
Residence address: ________
Post Office address: ________

Co-Inventor's signature : ________ **date :** ________
Co-Inventor's printed full name: ________ **Citizenship:** ________
Employee #: ____ **Extension:** ____ **Mail stop:** ____ **Home telephone:(** **)** ____
Division: ____ **Directorate:** ____ **Dept #:** ____ **Dept :** ____ **Manager:** ____
Residence address: ________
Post Office address: ________
List on additional sheet if there are more co-inventors and list total number of inventors here: ____

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known:
LAW FIRM: RENNER, OTTO, BOISSELLE & SKLAR
LAWYERS: David Galin and Andrew Romero

Witness 1 initial: ________ **Witness 2 initial:** ________

[redacted]

AMD CONFIDENTIAL

PAGE 6/13 * RCVD AT 1/8/2004 2:19:55 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):04-28

TDG—SOI PATENT HARVESTING SESSION

[redacted]

INITIAL LIST OF PARTICIPANTS
GROUP 1: ROOM C-3
TOPIC: SOI Devices
LAW FIRM: Renner, Otto, Boisselle & Sklar (David Galin and Andrew Romero)
Technical Leader: Srinath Krishnan

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Ralf vanBentum Ralf.vanBentum@amd.com NOTE: Ralf will be in the USA for 3 months, then he will return to AMD's ffices in DRESDEN, GERMANY—E-mail will be useful for getting Dresden address.	GERMANY	0201279	07882	79	408/749-3293	408/749-3851	1220 North Fair Oaks Avenue, #1214	Sunnyvale	CA	94089
Yu, Bin Bin.Yu@amd.com	CHINA	024313	07360	143	408/749-2147	408/749-5585	1373 Poppy Wy	Cupertino	CA	95014

PAGE 1A

AMD INVENTION DISCLOSURE

TLD ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

Identify known relevant art (patents, publications, products): _____

State the problem solved by this invention: Improving Ioff while maintaining high Ion

Brief description and/or sketch of invention (*please attach copies of AMD patent notebook pages, reports or drawings*):

The thin metal oxide and nitride layer on the sidewall of metal gate enable us that workfunction of the gate itself and poly spacers are uniquely defined. Poly spacers and metal gate are connected at the top to share the same load voltage.

The workfunction of poly spacer is 0.3–0.5eV less the metal gate, thus it inverts the channel before the metal gate.

The device acts like a much longer channel device in the off state (low Ioff) and as short channel in the on state (high Ion)

Patent notebook # _____ Page numbers _____ Number of drawings _____

Witness 1 initial: _____ Witness 2 initial: _____

[redacted] AMD CONFIDENTIAL Page 2

AMD INVENTION DISCLOSURE

TLD ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS68. Texas x55964 return to MS562

Advantages (check all that apply):

☐ avoids existing patent(s)	☐ improves precision	☐ simplifies manufacturing
☑ new function	☐ improves accuracy	☐ improves wear characteristic
☐ improves density	☐ improves efficiency	☐ improves signal to noise ratio
☑ increases operating speed	☐ fewer component parts	☐
☐ improves reliability	☐ reduces cost of manufacturing	☐

Discussion of advantage of the invention over other solutions
(*emphasize technical advance in the art* as measured against known art):_____

an FDSOI device with very low Ioff

First written description* of invention, date: 7/28/01	First external disclosure to (name):
Date of first drawing*: Date invention first reduced to practice:	Date of first external disclosure, none ☐ External disclosure under NDA* No ☐ Yes ☐
Made by (name): Tested by (name):	First external disclosure or use by: presentation ☐, announcement ☐, sample ☐, sale ☐, other ☐
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
any of above occurred outside of USA ☐	Publication name:
* *attach copy if possible*	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when?_____
Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No ☑, Yes ☐. If yes, company name_____
If yes, name of AMD business contact and contract no._____
Was invention jointly developed with participation of inventors from outside AMD: No ☑ Yes ☐.
If yes, Company name_____

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature:_____ **Date:**_____
Printed name:_____ **Employee #:**_____

Witness 2 signature:_____ **Date:**_____
Printed name:_____ **Employee #:**_____

*After completing to this point, deliver to department reviewer: date delivered*_____

Witness 1 initial:_____ **Witness 2 initial:**_____

AMD INVENTION DISCLOSURE

TLD ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

DISCLOSURE EVALUATION (*Entries from this point on are by the Reviewer*)

Does this invention add value to the AMD intellectual property portfolio? Yes ☐, No ☐,
Explain:_____

Do you know of any relevant art? Yes ☐, No ☐, If yes, attach a copy and explain: _____

What application(s) do you foresee for this invention? _____

I estimate the Value* of this invention disclosure is **A** ☐, **B** ☐, **C** ☐, **D** ☐,
** use worksheet "Valuing Invention Disclosures and Patents".*

it is ☐, is not ☐ recommended to AMD for U.S. patent application filing,
it is ☐, is not ☐ recommended to AMD for foreign patent application filing,
it is ☐, is not ☐ recommended to be held as an AMD trade secret,
Give this high priority ☐, normal ☐, low priority ☐, in patent application writing.

GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION
Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.
ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:

- ***Invention is High-Valued (A, B)*, and***
- ***Invention is in our technology path (usage), and***
- ***Invention usage is detectable by inspection of product, and***
- ***Invention is relatively hard to design around, and***
- ***Competitor is operating in the country of interest. (see ca000000.xls tabulation of "Factory Sites outside the USA .)***

I recommend filing patent applications in foreign countries checked below:

Japan ☐	S.Korea ☐	Taiwan ☐	U.K. ☐	France ☐	Germany ☐
☐	☐	☐	☐	☐	☐

Reviewer's signature:_____ **Employee #:**_____ **Date:**_____

Reviewer's printed name: _____ If foreign filing is checked, route to *Div. VP* for signature.

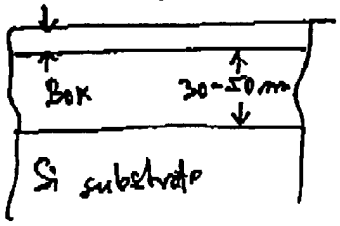
VP or Designate approves foreign filing (signature)_____

Reviewer: Complete this page and send disclosures to TLD for patent application filing.

Straddled gate FDSOI

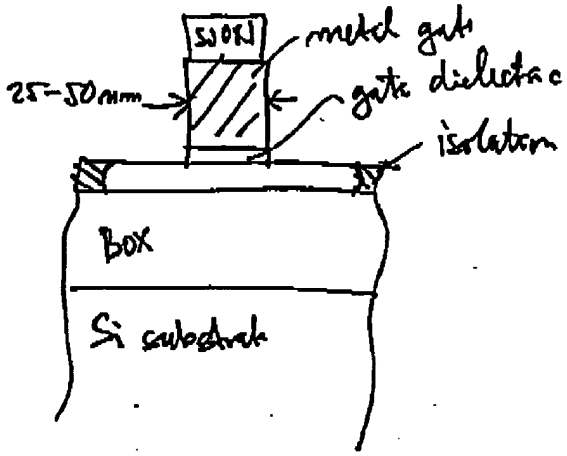
Flow:

5-15 nm superficial silicon (undoped)

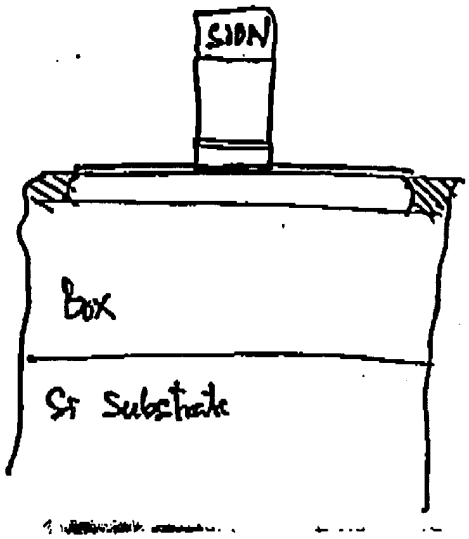


The thin superficial silicon layer is oxidized to form LOCOS-type isolation.

After deposition of high k material (ZrO_2, HfO_2, Ta_2O_5, etc.) with an equivalent oxide thickness of 1 nm we deposit 50-70 nm tungsten and pattern it

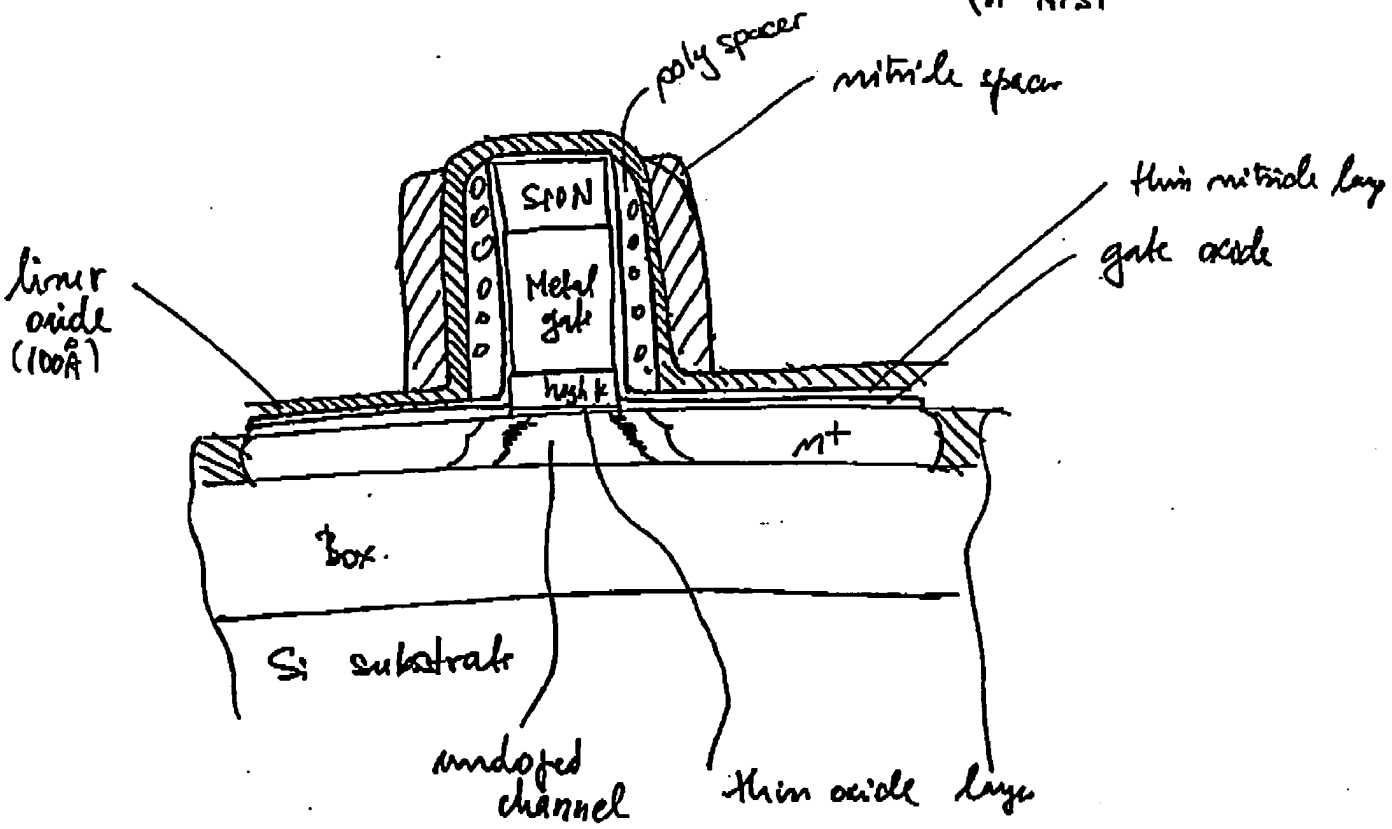


Next we do a short oxidation (at 800-900° C) to grow ~ 10-12 Å of oxide on exposed silicon. Oxidation is followed by thin nitride deposition (~10 Å). During oxidation the sidewall of the gate can form metallic oxides and it is also covered by nitride. There is also a thin layer of silicon dioxide underneath the high k dielectric.



Straddled gate FDSOI/page 2

After poly deposition (150-250 Å) we form poly spacers (param, next page) we implant shallow extensions (As: 1-5 e14 @ 2-4 keV).
Next we deposit 100 Å oxide and 300 - 500 Å nitride and form spacer, followed by source/drain implant (As: 2-4 e15, 15-25 keV) and RTA anneal (5-10" @ 1000 - 1020°C). or Ti: 2-4 e15, 10-15 keV) for NiSi



Polysilicon spacer get doped during the implants. The junction should just barely reach under the poly spacer (the previous junction is wrong and thus crossed over).

Next we open the source/drain area by removing liner oxide and thin nitride and oxide layers. At the same time we also expose the top of poly spacers and then selective grow 150-200 Å of Si.

Next we deposit Co or Ni and form silicide. After TEOS deposition (3500-4500 Å) we polish it back to stop on SiON and Si_3N_4 layers. During this polishing SiON protects metal gate from dishing.

Next we remove SiON layer. During this process we also remove a part of nitride spacer.

Next we open source and drain contacts, deposit diffusion barrier (TiN) and form contact plugs.